ABSTRACT OF THE DISCLOSURE

The liquid crystal display device includes a MLA operating circuit which reads from gradation data of [b2, b1, b0] stored in frame memories b2 in a period of the first frame, and b1 and b0 in periods T1 and T0 of the second frame to produce a column data signal 104([c2, c1,c0]), and a timing control circuit which controls a latch signal to column drivers so that the time ratio of the first frame to the second frame is 4:3 and the time ration of divided selection periods in the second frame is 2:1. With this, the number of change points of voltage level applicable in selection periods can be reduced whereby occurrence of a waveform distortion is minimized and a possibility of an uneven display in the liquid crystal display device is reduced.